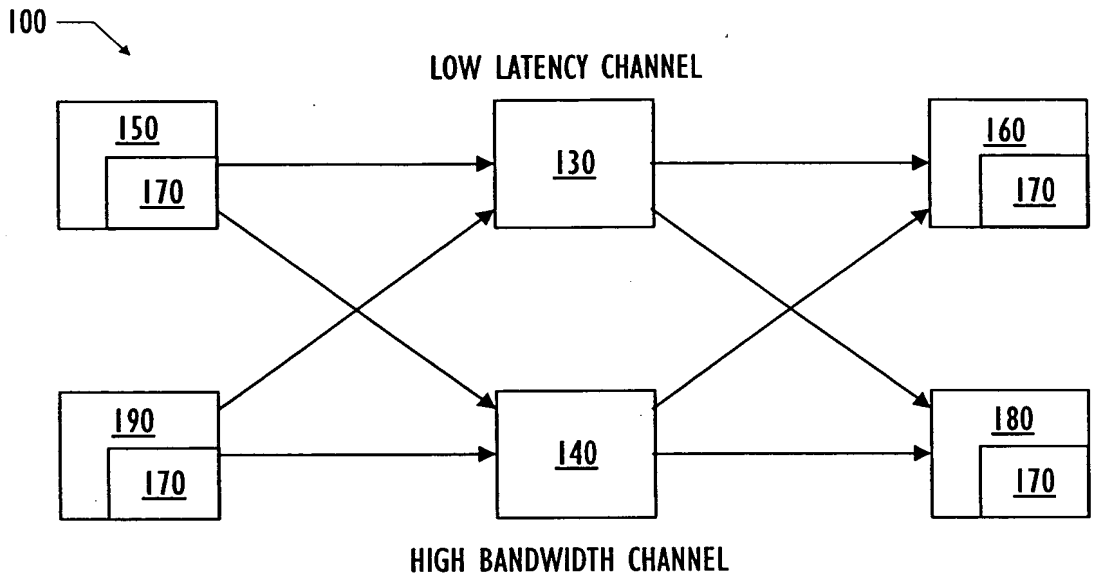


FIG. 1

09/2020 EAST Version: 4.0.1.0

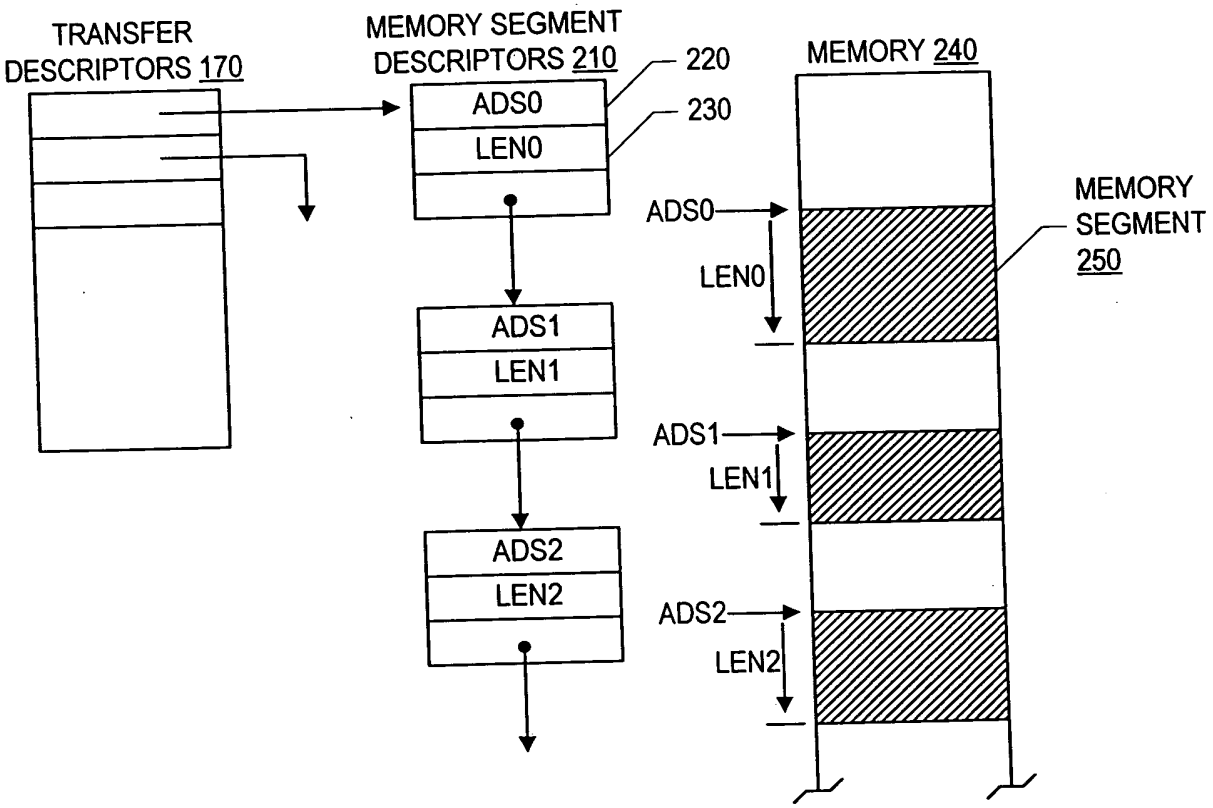

TRANSFER
DESCRIPTORS 170
MEMORY SEGMENT
DESCRIPTORS 210
220
230
ADS0
LEN0
ADS1
LEN1
ADS2
LEN2
MEMORY 240
MEMORY
SEGMENT
250
ADS0
LEN0
ADS1
LEN1
ADS2
LEN2

FIG. 2

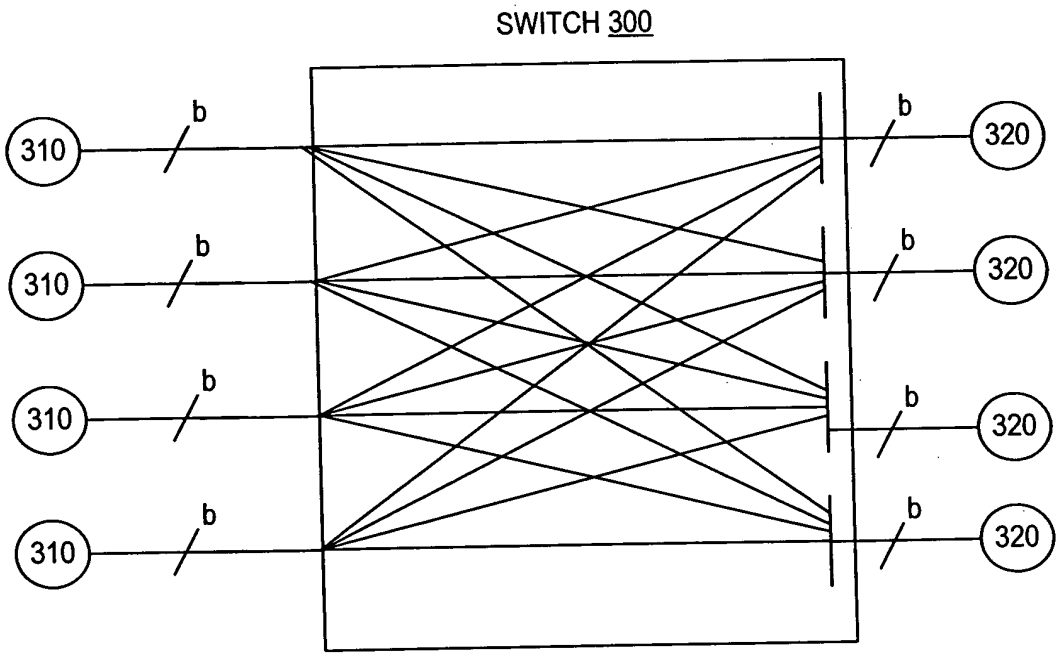


FIG. 3

Docket No. 21006/US

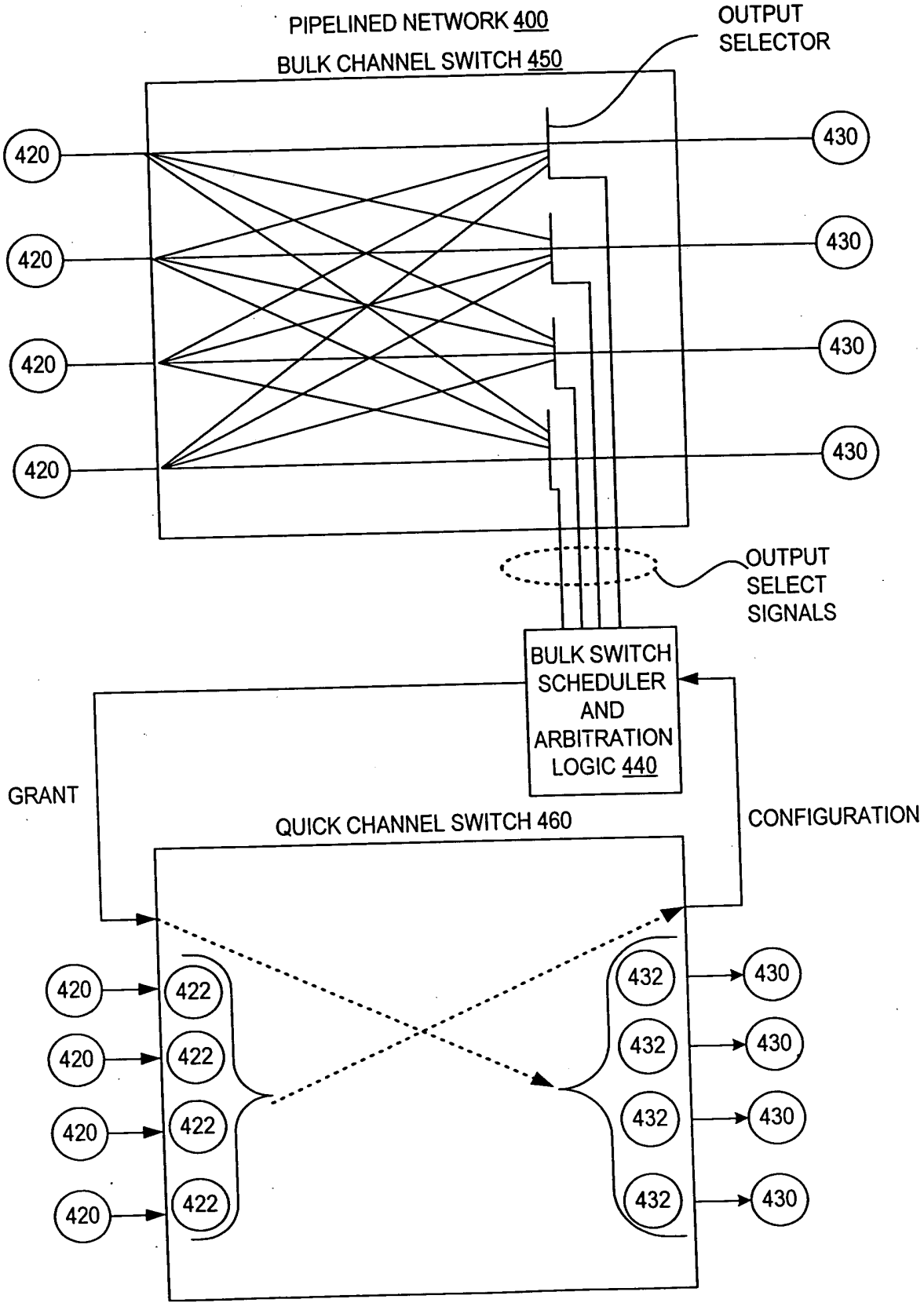

PIPELINED NETWORK 400
BULK CHANNEL SWITCH 450
OUTPUT SELECTOR
420
420
420
420
430
430
430
430
OUTPUT SELECT SIGNALS
BULK SWITCH SCHEDULER AND ARBITRATION LOGIC 440
GRANT
CONFIGURATION
QUICK CHANNEL SWITCH 460
420
420
420
420
422
422
422
422
432
432
432
432
430
430
430
430

FIG. 4

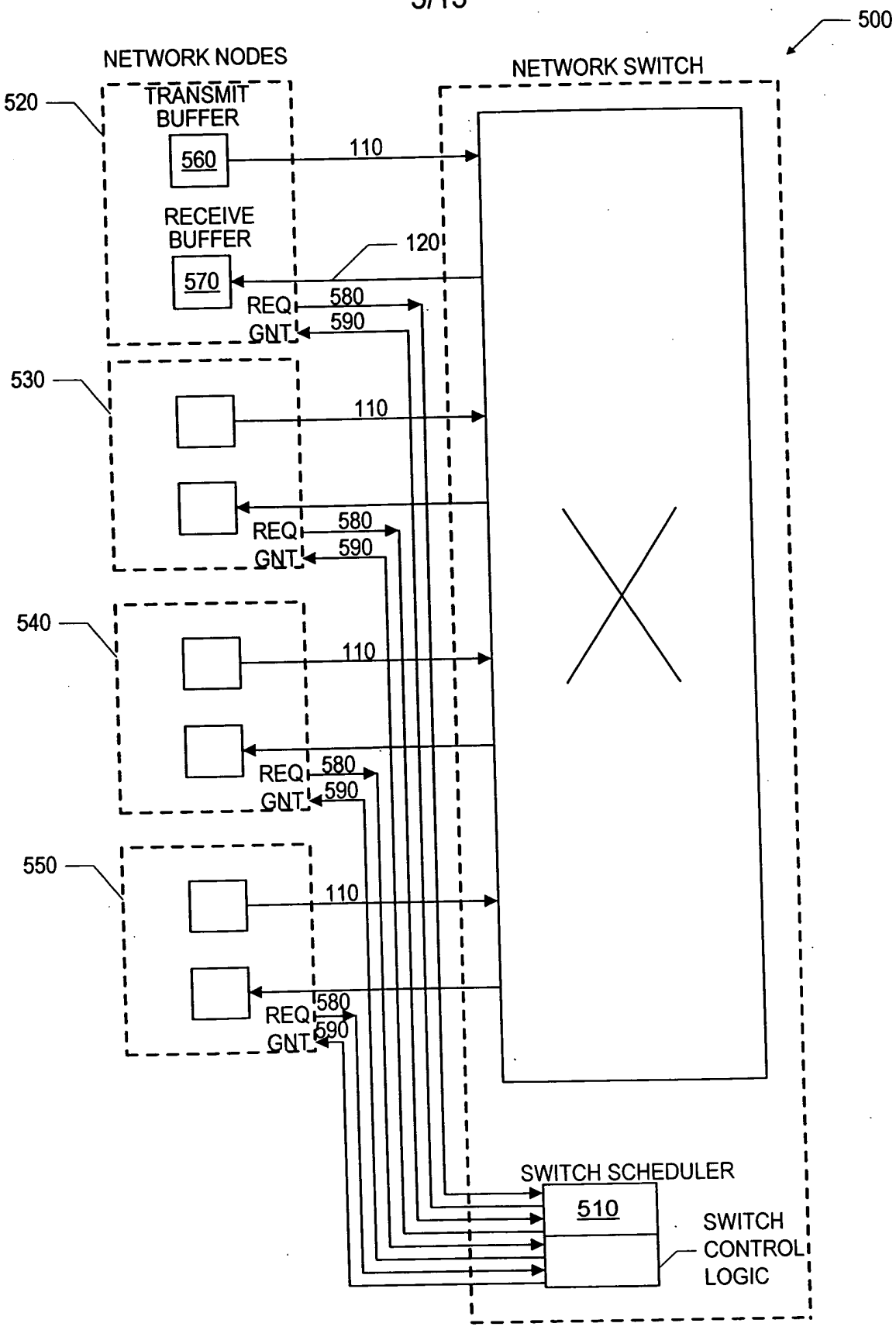

500
NETWORK NODES
NETWORK SWITCH
520
TRANSMIT BUFFER
560
110
RECEIVE BUFFER
570
120
REQ
580
GNT
590
530
110
REQ
580
GNT
590
540
110
REQ
580
GNT
590
550
110
REQ
580
GNT
590
SWITCH SCHEDULER
510
SWITCH CONTROL LOGIC

FIG. 5

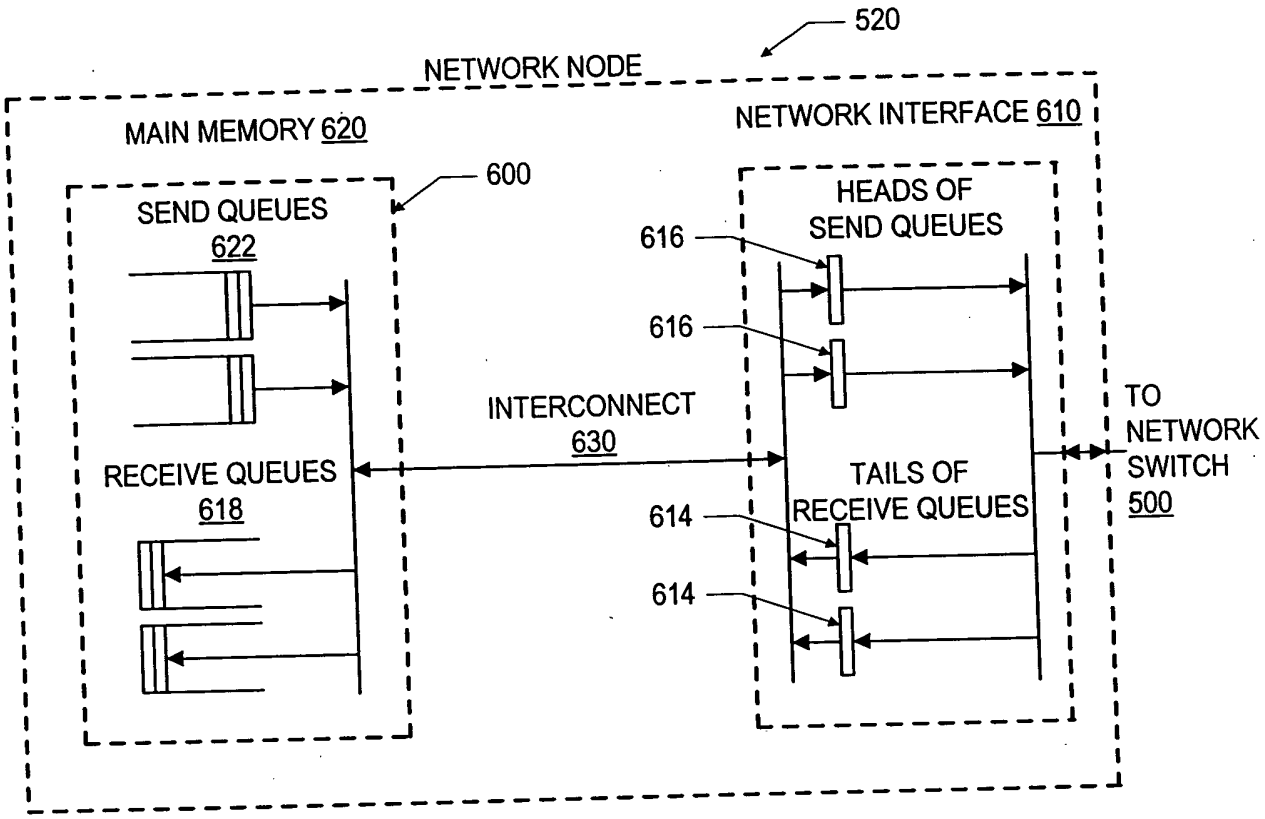


FIG. 6

Docket No. 50325-2000

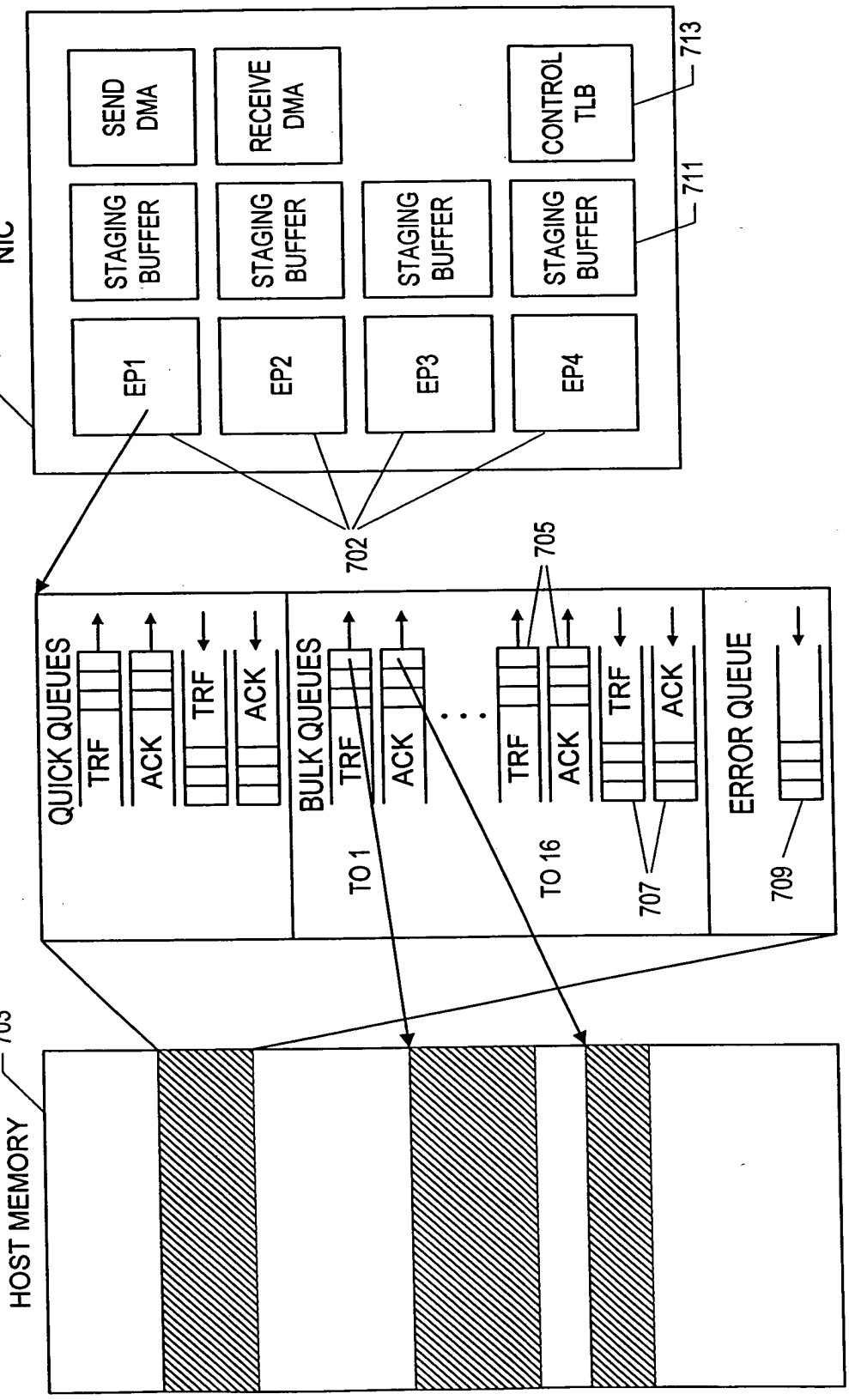

NIC
701
SEND DMA
RECEIVE DMA
CONTROL TLB
713
STAGING BUFFER
STAGING BUFFER
STAGING BUFFER
STAGING BUFFER
711
EP1
EP2
EP3
EP4
700
702
705
QUICK QUEUES
TRF
ACK
TRF
ACK
BULK QUEUES
TRF
ACK
TRF
ACK
TRF
ACK
TO 1
TO 16
707
ERROR QUEUE
709
HOST MEMORY
703

FIG. 7

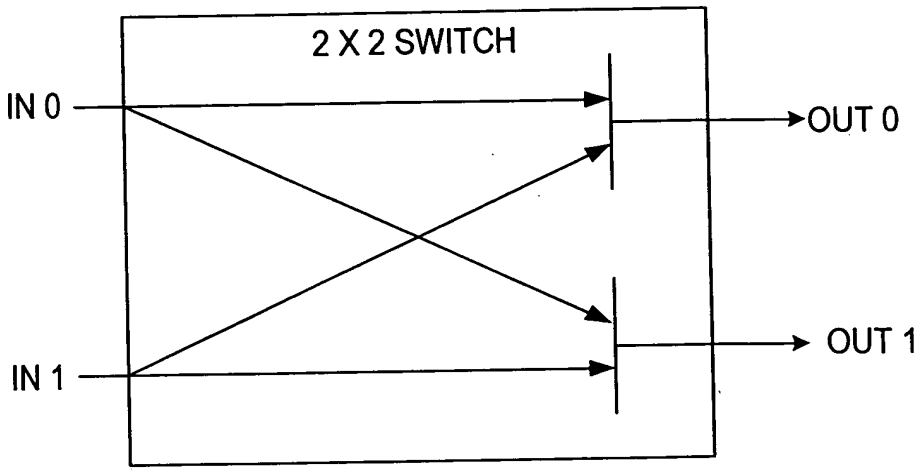


FIG. 8

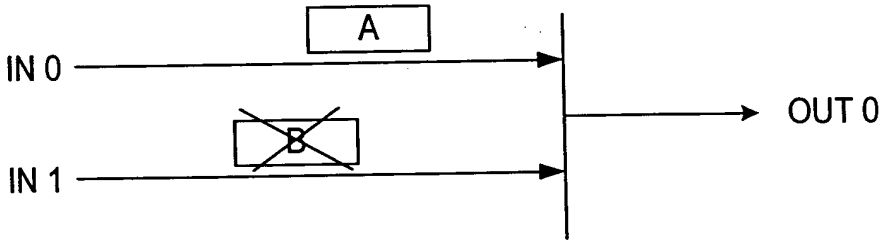


FIG. 9A

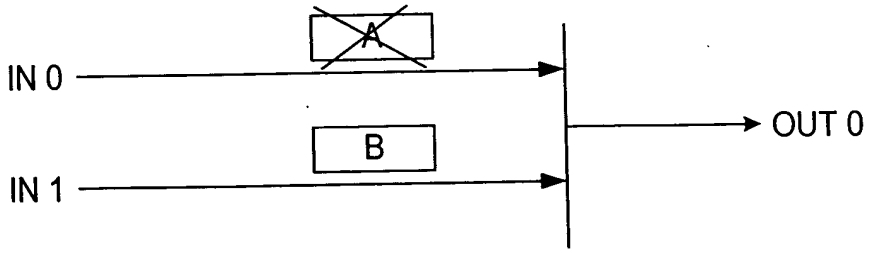


FIG. 9B

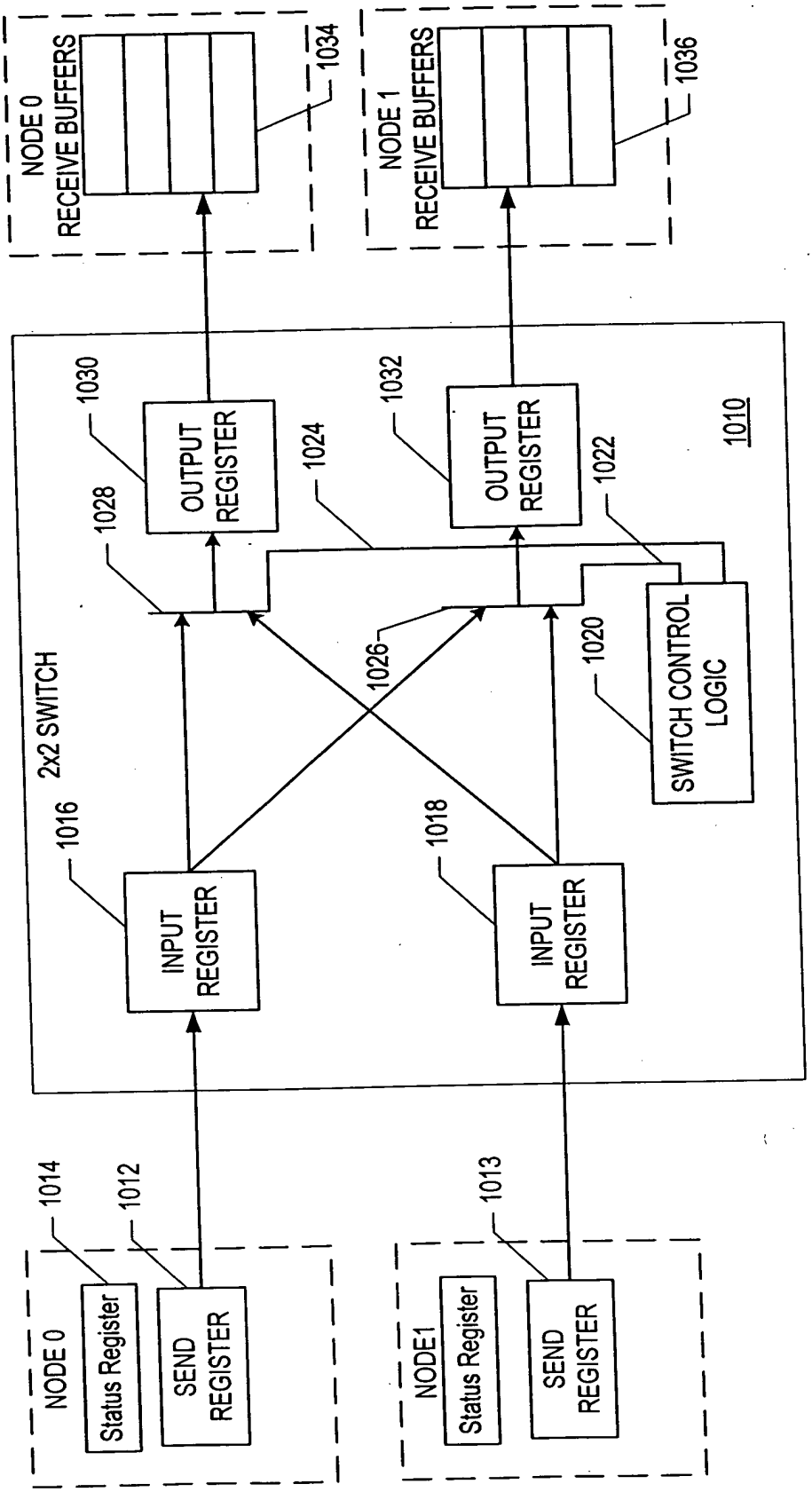

NODE 0
RECEIVE BUFFERS
1034
NODE 1
RECEIVE BUFFERS
1036
1030
OUTPUT REGISTER
1032
OUTPUT REGISTER
1024
1028
1022
2x2 SWITCH
1010
1026
1020
SWITCH CONTROL LOGIC
1016
INPUT REGISTER
1018
INPUT REGISTER
NODE 0
1014
Status Register
1012
SEND REGISTER
NODE1
1013
Status Register
SEND REGISTER

FIG. 10

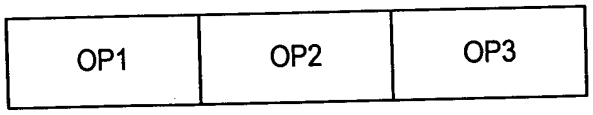


FIG. 11A

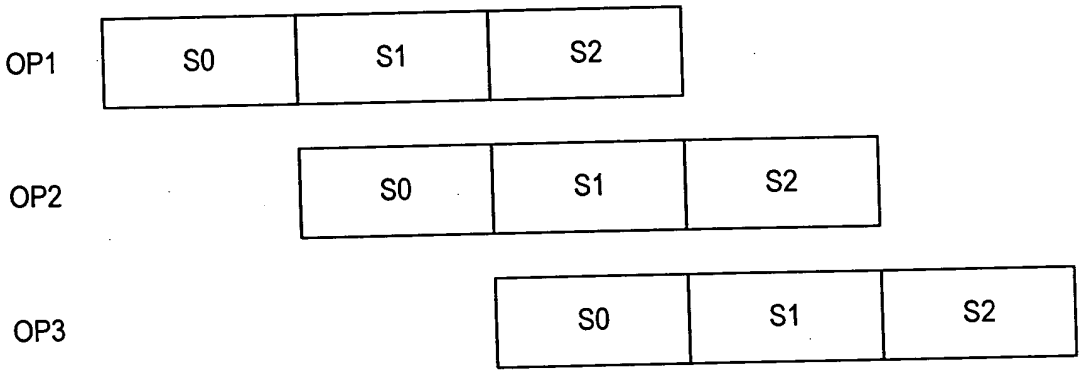


FIG. 11B

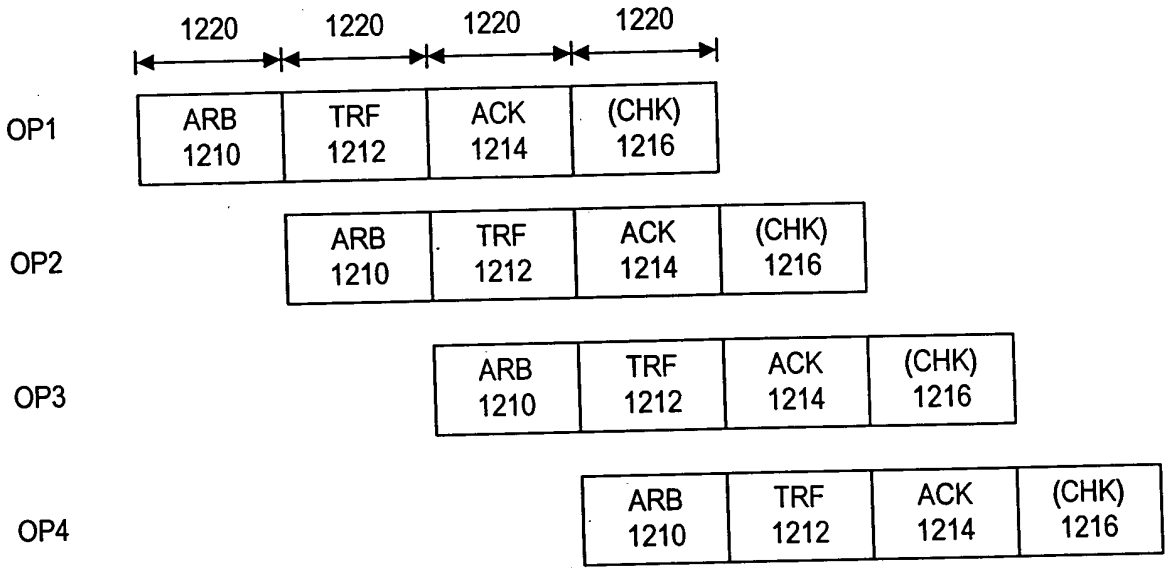
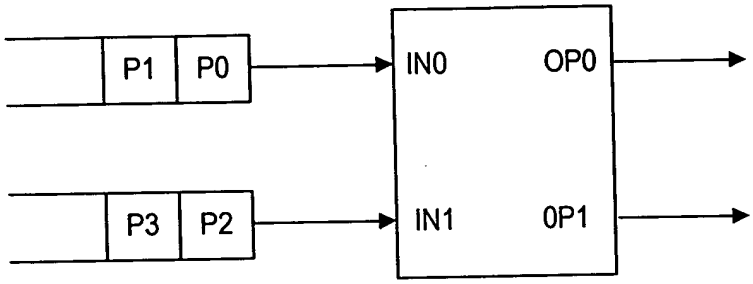

1220
1220
1220
1220
OP1
ARB 1210
TRF 1212
ACK 1214
(CHK) 1216
OP2
ARB 1210
TRF 1212
ACK 1214
(CHK) 1216
OP3
ARB 1210
TRF 1212
ACK 1214
(CHK) 1216
OP4
ARB 1210
TRF 1212
ACK 1214
(CHK) 1216

FIG. 12



PACKETS P0, P2 ARE DESTINED FOR O0
PACKETS P1, P3, ARE DESTINED FOR O1

FIG. 13

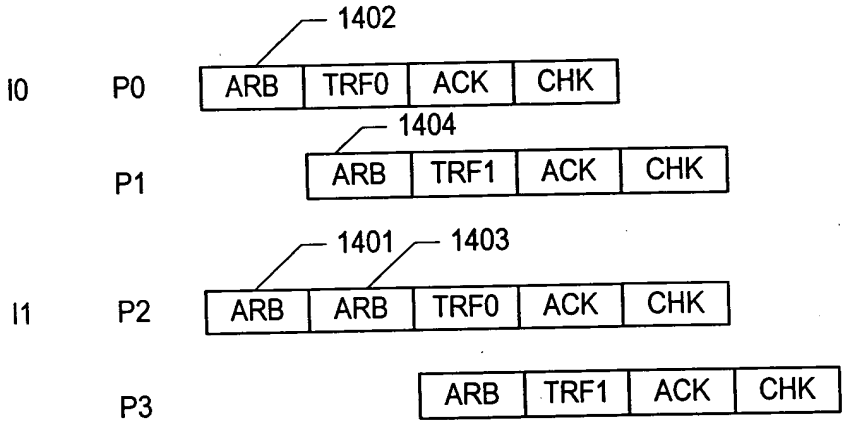


FIG. 14

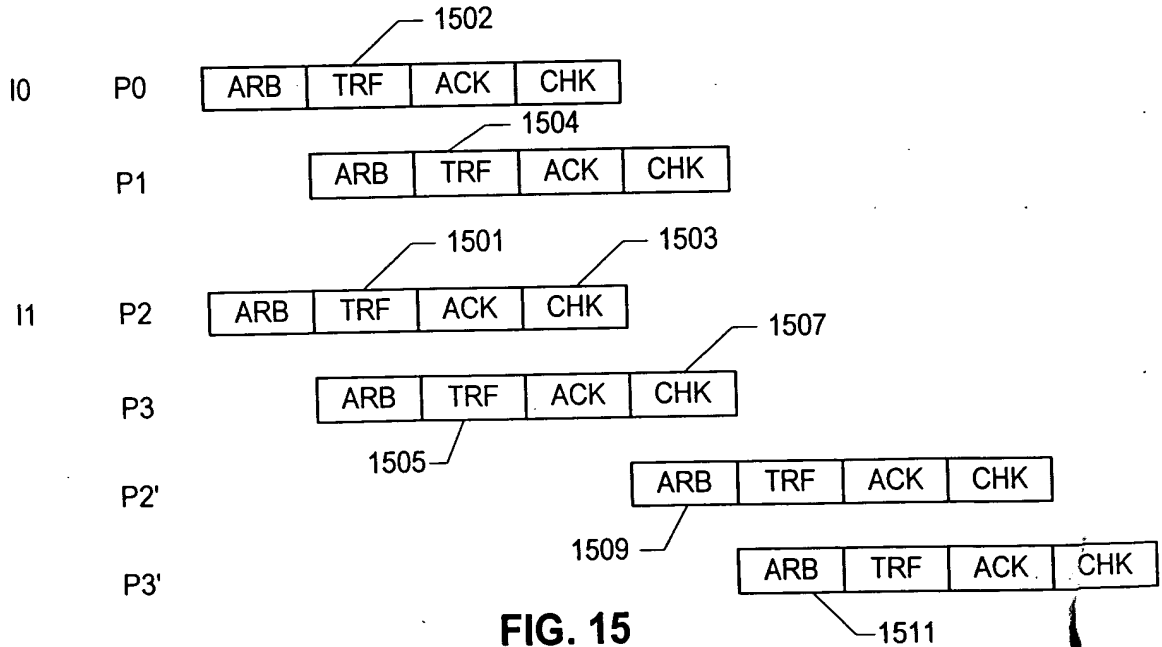


FIG. 15

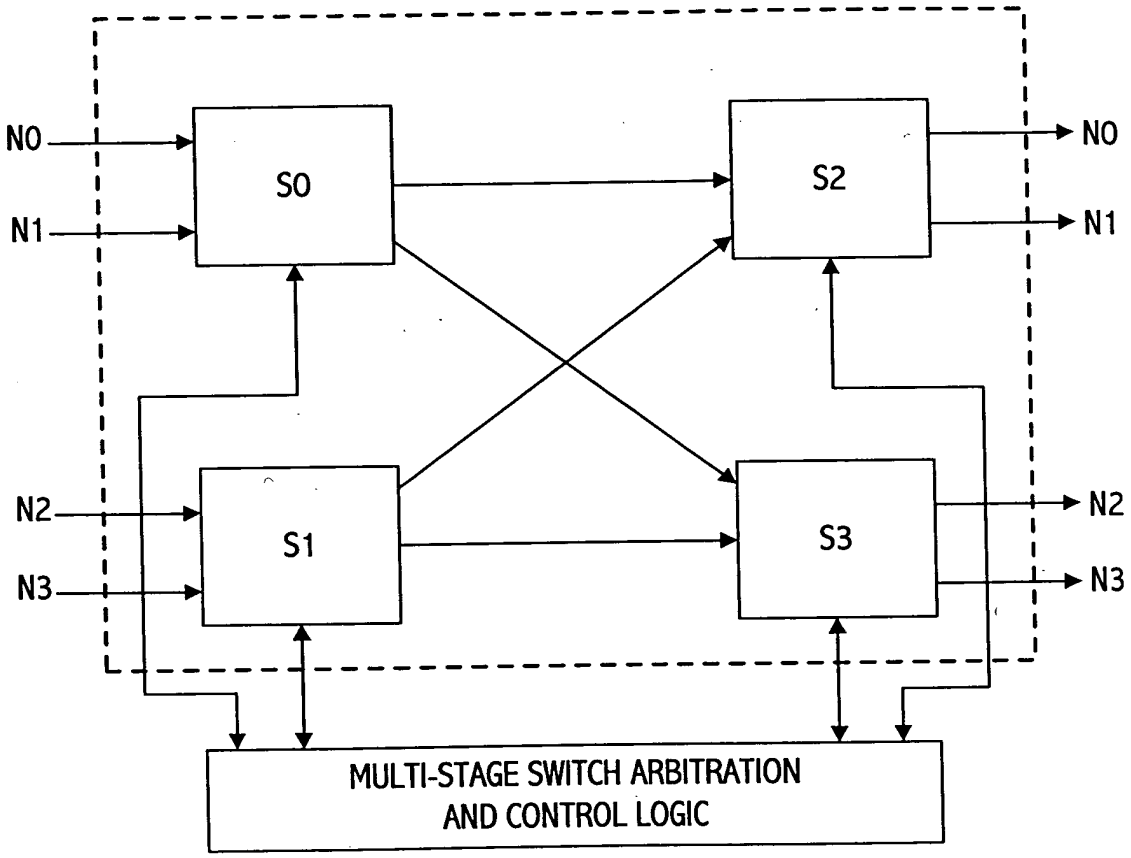

N0
N1
N2
N3
S0
S1
S2
S3
N0
N1
N2
N3
MULTI-STAGE SWITCH ARBITRATION
AND CONTROL LOGIC

FIG. 16